IN THE CLAIMS:

Please **amend** claims 1, 2 and 22, as follows:

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1. (Twice Amended) A semiconductor integrated circuit device comprising: a semiconductor substrate of a first conductivity type; a zener diode comprised of a first semiconductor region of a second conductivity type formed in a primary face of said semiconductor substrate, and a second semiconductor region of said first conductivity type formed in said semiconductor substrate at a bottom portion of said first semiconductor region and being smaller in area, defined by a planar pattern thereof, than said first semiconductor region,

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wherein a plurality of first connection holes for electrically connecting said first semiconductor region and a wire to each other are arranged in a region located outside a junction formed between said first semiconductor region and said second semiconductor region.

2. (Amended) A semiconductor integrated circuit device according to claim 1, wherein said second semiconductor region is arranged substantially at a center location of said first semiconductor region, and said plurality of first connection holes are arranged at a periphery of said first semiconductor region.

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22. (Amended) A semiconductor integrated circuit device according to claim 2, wherein a junction depth of said first semiconductor region in a region in which said first and second semiconductor regions form a PN junction is shallower than that of said first semiconductor region in a region in which said semiconductor substrate and said first semiconductor region form a PN junction.

Please **cancel** claims 12-14 without prejudice or disclaimer, while reserving applicants right to subsequently file a divisional application directed thereto and **insert** new claims 24-36, as follows:

24. A semiconductor integrated circuit device according to claim 3, wherein said second semiconductor region has an impurity concentration higher than that of said semiconductor substrate.

25. A semiconductor integrated circuit device according to claim 24, wherein a first conductivity type well region is formed on said semiconductor substrate, said first and second semiconductor regions are formed in said well region, said second semiconductor region has an impurity concentration higher than that of said well region, a wire is formed over said semiconductor substrate through

an insulation film, and said first connection holes are formed in the insulation film, respectively.

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26. A semiconductor integrated circuit device according to claim 1, wherein said second semiconductor region has an impurity concentration higher than that of said semiconductor substrate.

27. A semiconductor integrated circuit device according to claim 22, wherein said second semiconductor region has an impurity concentration higher than that of said semiconductor substrate.

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28. A semiconductor integrated circuit device according to claim 27, wherein a first conductivity type well region is formed on said semiconductor substrate, said first and second semiconductor regions are formed in said well region, said second semiconductor region has an impurity concentration higher than that of said well region, a wire is formed over said semiconductor substrate through an insulation film, and said first connection holes are formed in the insulation film, respectively.

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29. A semiconductor integrated circuit device comprising:

a first semiconductor region of a first conductivity type in a semiconductor substrate;

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a second semiconductor region of a second conductivity type, the second semiconductor region being formed on said first semiconductor region;

a third semiconductor region of a first conductivity type, the third semiconductor region being formed over said first semiconductor region and under said second semiconductor region; and

an insulation film formed over a primary face of said semiconductor substrate and having a plurality of first connection holes for electrically connecting therethrough said second semiconductor region and wiring,

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wherein a PN junction formed between said second semiconductor region and said third semiconductor region functions as a diode device, said third semiconductor region has an impurity concentration higher than that of said first semiconductor region, said second semiconductor region has a first portion and a second portion, the first portion is that in which a PN junction is formed between said third semiconductor region and said second semiconductor region and the second portion is that below which said third semiconductor region is not formed, a junction depth of said first portion is shallower than that of said second portion, said second portion is formed outside said first portion, and said first connection holes are formed over said second portion of said second semiconductor region.

30. A semiconductor integrated circuit device according to claim 29, wherein said diode device constitutes a zener diode.

31. A semiconductor integrated circuit device according to claim 29, wherein said second portion is formed in a periphery of said first portion so as to surround said first portion, and said plurality of first connection holes are arranged over said second portion so as to surround said first portion.

32. A semiconductor integrated circuit device comprising:

a first semiconductor region of a first conductivity type, the first semiconductor region being formed over a semiconductor substrate;

a second semiconductor region of a second conductivity type, the second semiconductor region being formed under said first semiconductor region; and

an insulation film formed over a primary face of said semiconductor substrate and having a plurality of first connection holes for electrically connecting therethrough said first semiconductor region and wiring,

wherein said first semiconductor portion has a first portion and a second portion, the first portion is that below which said second semiconductor region is formed and

the second portion is that below which said second semiconductor region is not formed, a PN junction is formed between said second semiconductor region and said first semiconductor region at said first portion and functions as a diode device, said second portion is formed outside said first portion, and said first connection holes are formed over said second portion of said first semiconductor region.

33. A semiconductor integrated circuit device according to claim 32, wherein the diode device constitutes a zener diode device.

34. A semiconductor integrated circuit device according to claim 33, wherein said second portion is formed in a periphery of said first portion so as to surround said first portion, and said plurality of first connection holes are arranged over said second portion so as to surround said first portion.

35. A semiconductor integrated circuit device according to claim 33, wherein a junction depth of said first portion of said first semiconductor region is shallower than that of said second portion of said second semiconductor region.

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36. A semiconductor integrated circuit device comprising:

a first conductivity type well region formed on a semiconductor substrate;

a first semiconductor region of a second conductivity type, the first semiconductor region being formed on said well region;

a second semiconductor region of a first conductivity type, the second semiconductor region being formed in said well region and under said first semiconductor region; and

an insulation film formed over a primary face of said semiconductor substrate and having a plurality of first connection holes for electrically connecting therethrough said first semiconductor region and wiring,

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wherein said second semiconductor region has an impurity concentration higher than that of said well region, said first semiconductor region has a first portion and a second portion, the first portion is that below which said second semiconductor region is formed and the second portion is that below which said semiconductor region is not formed, a PN junction is formed between said second semiconductor region and said first semiconductor region at said first portion and constitutes a zener diode, a junction depth of said first portion is shallower than that of said second portion, said second portion is formed in a periphery of said first portion so as to surround said first portion, and

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said plurality of first connection holes are arranged over said second portion so as to surround said first portion.